


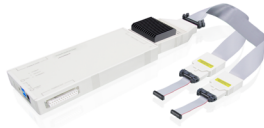



# Microprocessor Off-Chip Trace Solutions Overview

	PowerTrace System				
					
	PowerTrace Serial 2	PowerTrace III	PowerTrace II Lite	CombiProbe 2	µTrace
<b>Application</b>	High-performance serial tracing	High-performance parallel tracing	Parallel tracing	Advanced debugging and system trace	All-in-one debug and trace solution
<b>Memory Size</b>	4 GB or 8 GB	4 GB or 8 GB	1 GB	512 MB	256 MB
<b>Maximum Bandwidth</b>	80 Gbit/s	19.2 Gbit/s	10.8 Gbit/s	3.2 Gbit/s	1.6 Gbit/s
<b>Streaming Performance</b>	400 Mbyte/s	400 Mbyte/s	100 Mbyte/s	140 Mbyte/s	140 Mbyte/s
<b>Parallel Trace<sup>1</sup></b>	—	Up to 36 signals 600+ Mbit/s per signal for 17 signals 350 Mbit/s per signal for 36 signals	Up to 36 signals 450 Mbit/s per signal for 17 signals 225 Mbit/s per signal for 36 signals	Two ports with up to 4 signals each. 400 Mbit/s per signal (for all signals)	One ports with up to 4 signals. 400 Mbit/s per signal (for all signals)
<b>Serial Trace<sup>2</sup></b>	Up to 8 lanes with 12.5 Gbit/s per lane Up to 4 lanes with 22.5 Gbit/s per lane <sup>4</sup>	Up to 4 lanes <sup>3</sup> 6.25 Gbit/s per lane for 3 lanes 5.00 Gbit/s per lane for 4 lanes	Up to 4 lanes <sup>13</sup> 6.25 Gbit/s per lane for 2 lanes 4.50 Gbit/s per lane for 3 lanes 3.38 Gbit/s per lane for 4 lanes	—	—
<b>Serial trace via PCIe</b>	PCIe2 / PCIe3: Up to 8 lanes PCIe4 <sup>4</sup> : Up to 4 lanes	—	—	—	—
<b>Supported Trace Protocols</b>	ETM, PTM, TWP, MCDS, Nexus, HSDP, AGBT, Aurora	ETM, PTM, TWP, SWV, MCDS, Nexus, STP	ETM, PTM, TWP, SWV, MCDS, Nexus, STP	ETM, TWP, SWV, MCDS, Nexus <sup>5</sup> , STP	ETM, TWP, SWV
<b>Optional Analog/Digital Probe</b>	Mixed Signal Probe (12 digital, 6 voltage, 2 current channels)	Mixed Signal Probe (12 digital, 6 voltage, 2 current channels)	—	Mixed Signal Probe <sup>6</sup> (12 digital, 6 voltage, 2 current channels)	Mixed Signal Probe (12 digital, 6 voltage, 2 current channels)
<b>Supported CPU Architectures</b>	More than 150 CPU architectures and sub-architectures				Arm® Cortex®-M / RISC-V 32-bit
<b>Required Base Module</b>	PowerDebug X51			PowerDebug E40 or PowerDebug X51	—
<b>Link</b>	<a href="#">view more</a>	<a href="#">view more</a>	<a href="#">view more</a>	<a href="#">view more</a>	<a href="#">view more</a>

<sup>1</sup> Requires trace preprocessor. Pin-count and recording-speed depends on used preprocessor and trace protocol.

<sup>2</sup> We specify here the speed of the serial link. The maximum speed for the transferred payload is usually smaller due to line encoding, e.g. 80 % with 8b/10b encoding.

<sup>3</sup> Requires serial preprocessor. For serial tracing we recommend PowerTrace Serial.

<sup>4</sup> Requires preprocessor.

<sup>5</sup> Nexus with CombiProbe only for RISC-V.

<sup>6</sup> Instead of 2nd trace port.